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09/606,730	06/29/2000	Paul C. Wilson	07072-105001	6692

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DALY, CROWLEY & MOFFORD, LLP
SUITE 101
275 TURNPIKE STREET
CANTON, MA 02021-2310

EXAMINER	
PUENTE, EMERSON C	

ART UNIT	PAPER NUMBER
2113	22

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/606,730	Applicant(s) WILSON ET AL.	
	Examiner Emerson C Puente	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,26,32-39,44-46 and 52-54* is/are allowed.

6)☒ Claim(s) *2-7,9,11-15,18,19,27,29-31,40-43 and 47-49* is/are rejected.

7)☒ Claim(s) *10,16,17,20-25,28,50 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *18* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim 1 was canceled. Claims 2-54 have been examined.

This action is made **Non-Final**.

Drawings

This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Objections

Claims 22-24, 50, and 51 are objected to because of the following informalities:

Claims 22-24 are identical to claim 14-16, respectively. Please cancel claims 22-24.

Claims 50 and 51 are identical to claim 32 and 34, respectively. Please cancel claims 50 and 51.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over US Patent No. 5,819,054 of Ninomiya et al. referred hereinafter "Ninomiya".

In regards to claim 2, Ninomiya's first teaching discloses a data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

a plurality of first directors coupled to the host computer/server (see figure 20 item 201 and column 1 lines 26-46);

a plurality of second directors coupled to the bank of disk drives (see figure 20 item 202 and column 1 lines 26-46);

a cache memory (see figure 20 item 203 and column 1 lines 26-46).

wherein there are separate point-to-point data paths between each one of the directors and the cache memory (see figure 20 items 207, 208 and column 1 lines 26-46).

Ninomiya's first teaching fails to explicitly disclose:

including a backplane and wherein the cache memory and directors are interconnected through the backplane

Ninomiya's secondary teaching discloses:

including a backplane and wherein the cache memory and directors are interconnected through the backplane (see figure 8 and column 8 lines 29-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a backplane and wherein the cache memory and directors are interconnected through the backplane. A person of ordinary skill in the art would have been motivated because Ninomiya first teaching discloses host adaptors, cache memory, and disk adaptors being connected (see figure 20) and a backplane, as per secondary teachings of Ninomiya, enables connection of the host adaptors, cache memory, and disk adaptors (see column 8 lines 29-41)

In regards to claim 3, Ninomiya secondary teaching discloses a system wherein the backplane is a printed circuit board (see figure 8 and column 8 lines 29-30).

Claims 2-7, 9,11-15,18,19,27, 29-31, 40-43, and 47-49 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over US Patent No. 5,214,768 of Martin in view of Ninomiya.

In regards to claims 2, 4, and 5, Martin discloses a data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

a plurality of first directors coupled to the host computer/server (see figure 1 items 14,16,18,19);

a plurality of second directors coupled to the bank of disk drives (see figure 1 item 48).

a message network coupled to the plurality of directors and the plurality of second directors(see figure 1 item 40 and column 7 lines 35-62), such first and second directors controlling data transfer between the host computer and the bank of disk drives in response to messages passing between the directors through the messaging network as such data passes through the memory via the data transfer section (see column 7 lines 63-68 and column 8 lines 1-18).

a data transfer section coupled to the plurality of first directors and the second directors (see figure 1 item 42).

wherein there are separate point-to-point data paths (see figure 1).

However, Martin fails to disclose a system interface comprising:

a cache memory ;

a data transfer section coupled to the cache memory;

wherein there are separate point-to-point data paths between each one of the directors and the global cache memory.

Ninomiya discloses a system interface comprising:

a cache memory (see figure 20 item 203 and column 1 lines 26-46).

a data transfer section coupled to the plurality of first directors, second directors, and cache memory (column 1 lines 26-46)

wherein there are separate point-to-point data paths between each one of the directors and the global cache memory (see figure 20 items 207, 208 and column 1 lines 26-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Martin such that the system interface comprises of a cache memory. A person of ordinary skill in the art would have been motivated to make the modification to Martin because Martin discloses performing read operations in a data storage retrieval system (see column 8 line 10) and having a cache memory, as per teachings of Ninomiya, would reduce read access time, thus providing a faster system.

Furthermore, Ninomiya's secondary teaching discloses:

including a backplane and wherein the cache memory and directors are interconnected through the backplane (see figure 8 and column 8 lines 29-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a backplane and wherein the cache memory and directors are interconnected through the backplane. A person of ordinary skill in the art would have been motivated because Ninomiya first teaching discloses host adaptors, cache memory, and disk adaptors being connected (see figure 20) and a backplane, as per secondary teachings of Ninomiya, enables connection of the host adaptors, cache memory, and disk adaptors (see column 8 lines 29-41)

In regards to claim 3 and 6, Ninomiya discloses a system wherein the backplane is a printed circuit board (see figure 8 and lines 29-30).

In regards to claim 7, Martin discloses a system wherein the messaging network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors. Martin discloses a control subsystem and switch subsystem (see figure 1 items 40, 42), which both could constitute as the messaging network, indicating a switch network having plurality of ports, each of the ports being coupled to a corresponding one of the plurality of first and second directors.

In regards to claim 9, Martin discloses a system interface comprising:

a plurality of first directors (see figure 1 item 14, 16, 18, and 19);

a plurality of second directors (see figure 1 item 48);

a messaging network(see figure 1 item 40), operative independently of the data transfer section(see figure 1 item 42), coupled to the plurality of first and second directors.

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network with such messages by-passing the data transfer section (see column 5 line 63-67 and 7 lines 63-68)

wherein there are separate point-to-point data paths (see figure 1).

However Martin fails to disclose:

such data transfer comprising passing data through the directors to the cache memory in the data transfer section

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory.

Ninomiya discloses:

such data transfer comprising passing data through the directors to the cache memory in the data transfer section (see figure 20 item 203 and column 1 lines 26-46);

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors (see figure 20 item 203 and column 1 lines 26-46);

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory (see figure 20 item 207,208 and column 1 lines 26-46) .

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Martin such that the system interface comprises of a cache memory. A person of ordinary skill in the art would have been motivated to make the modification to Martin because Martin discloses performing read operations in a data storage retrieval system (see column 8 line 10) and having a cache memory, as per teachings of Ninomiya, would reduce read access time, thus providing a faster system.

In regards to claims 11-13, Martin discloses a system interface comprising:

a plurality of first directors (see figure 1 item 14, 16, 18, and 19);

a plurality of second directors (see figure 1 item 48);

a messaging network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors coupled to a corresponding one of the plurality of first and second directors (see figure 1 item 40,42);

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network with such messages by-passing the data transfer section (see column 5 line 63-67 and column 7 lines 63-68)

wherein there are separate point-to-point data paths (see figure 1).

However Martin fails to disclose:

such data transfer comprising passing data through the directors to the cache memory in the data transfer section

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory.

Ninomiya discloses:

such data transfer comprising passing data through the directors to the cache memory in the data transfer section (see figure 20 item 203 and column 1 lines 26-46);

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors (see figure 20 item 203 and column 1 lines 26-46);

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory (see figure 20 item 207,208 and column 1 lines 26-46) .

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Martin such that the system interface comprises of a cache memory. A person of ordinary skill in the art would have been motivated to make the modification to Martin because Martin discloses performing read operations in a data storage retrieval system (see column 8 line 10) and having a cache memory, as per teachings of Ninomiya, would reduce read access time, thus providing a faster system.

Claim14 is rejected under same rationale as claim 9

In regards to claim 15, Martin discloses wherein each one of the directors includes:

a data pipe coupled between an input of such one of the directors and the cache memory (see figure 3 item 138,140,142, and 144 and column 10 lines 46-62);

a controller for transferring the messages between the message network and such one of the directors (see column 6 lines 7-11)

Claim 18 is rejected under same rationale as claim 9

Claim 19 is rejected under same rationale as claim 15

Claim 27 is rejected under same rationale as claim 9.

Claims 29-30 are rejected under same rationale as claim 13.

In regards to claims 31, Martin discloses a system interface comprising:

a plurality of directors (see figure 1 item 14, 16, 18, 19, and 48);

a messaging network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors coupled to a corresponding one of the plurality of first and second directors (see figure 1 item 40,42);

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network with such messages by-passing the data transfer section (see column 5 line 63-67 and column 7 lines 63-68)

wherein the messaging network passes the messages from any of the plurality of directors to a selected one of the plurality of directors (see column 8 lines 10-20).

wherein there are separate point-to-point data paths (see figure 1).

However Martin fails to disclose:

such data transfer comprising passing data through the directors to the cache memory in the data transfer section

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory.

Ninomiya discloses:

such data transfer comprising passing data through the directors to the cache memory in the data transfer section (see figure 20 item 203 and column 1 lines 26-46);

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors (see figure 20 item 203 and column 1 lines 26-46);

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory (see figure 20 item 207,208 and column 1 lines 26-46) .

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Martin such that the system interface comprises of a cache memory. A person of ordinary skill in the art would have been motivated to make the modification to Martin because Martin discloses performing read operations in a data storage retrieval system (see column 8 line 10) and having a cache memory, as per teachings of Ninomiya, would reduce read access time, thus providing a faster system.

In regards to claims 40, Martin discloses a system interface comprising:

a plurality of first directors coupled to the host computer/server (see figure 1 item 14, 16, 18, 19);

a plurality of second directors coupled to the bank of disk drives (see figure 1 item 48);

a messaging network coupled to the plurality of first directors and the second directors (see figure 1 item 40,42), such first and second directors control data transfer between the host computer and bank of disk drives in response to messages passing between the directors through the messaging network as such data passes through the memory via the data transfer section (see column 7 lines 63-68 and column 8 lines 1-18)

wherein the messaging network passes the messages from any of the first plurality of directors to a selected one of said second plurality of directors and from any one of the second plurality of directors to a selected one of the first plurality of directors (see column 8 lines 10-20).

wherein there are separate point-to-point data paths (see figure 1).

However Martin fails to disclose:

such data transfer comprising passing data through the memory via the data transfer section

a data transfer section coupled to the plurality of first directors, the second directors, and the cache memory

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory.

Ninomiya discloses:

such data transfer comprising passing data through the memory via the data transfer section (see figure 20 item 203 and column 1 lines 26-46);

a data transfer section coupled to the plurality of first directors, the second directors, and the cache memory (see figure 20 item 203 and column 1 lines 26-46);

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory (see figure 20 item 207,208 and column 1 lines 26-46) .

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Martin such that the system interface comprises of a cache memory. A person of ordinary skill in the art would have been motivated to make the modification to Martin because Martin discloses performing read operations in a data storage retrieval system (see column 8 line 10) and having a cache memory, as per teachings of Ninomiya, would reduce read access time, thus providing a faster system.

In regards to claim 41, Martin in view of Ninomiya's first teaching fails to disclose;

including a backplane and wherein the cache memory and directors are interconnected through the backplane

However, Ninomiya's secondary teaching discloses:

including a backplane and wherein the cache memory and directors are interconnected through the backplane (see figure 8 and column 8 lines 29-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a backplane and wherein the cache memory and directors are interconnected through the backplane. A person of ordinary skill in the art would have been motivated because Ninomiya first teaching discloses host adaptors, cache memory, and disk adaptors being connected (see figure 20) and a backplane, as per secondary teachings of Ninomiya, enables connection of the host adaptors, cache memory, and disk adaptors (see column 8 lines 29-41)

In regards to claim 42, Ninomiya discloses a system wherein the backplane is a printed circuit board (see figure 8 and lines 29-30).

In regards to claim 43, Martin discloses a system wherein the messaging network comprises a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first and second directors. Martin discloses a control subsystem and switch subsystem (see figure 1 items 40, 42), which both could constitute as the

messaging network, indicating a switch network having plurality of ports, each of the ports being coupled to a corresponding one of the plurality of first and second directors.

In regards to claims 47, Martin discloses a system interface comprising:

a plurality of first directors (see figure 1 item 14, 16, 18, 19);

a plurality of second directors (see figure 1 item 48);

a messaging network coupled to the plurality of first directors and the second directors (see figure 1 item 40,42);

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network with such messages by-passing the data transfer section (see column 5 line 63-67 and 7 lines 63-68)

wherein the messaging network passes the messages from any of the first plurality of directors to a selected one of said second plurality of directors and from any one of the second plurality of directors to a selected one of the first plurality of directors (see column 8 lines 10-20).

wherein there are separate point-to-point data paths (see figure 1).

However Martin fails to disclose:

such data transfer comprising passing data through the memory via the data transfer section

a data transfer section coupled to the plurality of first directors, the second directors, and the cache memory

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory.

Ninomiya discloses:

such data transfer comprising passing data through the memory via the data transfer section (see figure 20 item 203 and column 1 lines 26-46);

a data transfer section coupled to the plurality of first directors, the second directors, and the cache memory (see figure 20 item 203 and column 1 lines 26-46);

and wherein there are separate point-to-point data paths between each one of the directors and the cache memory (see figure 20 item 207,208 and column 1 lines 26-46) .

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Martin such that the system interface comprises of a cache memory. A person of ordinary skill in the art would have been motivated to make the modification to Martin because Martin discloses performing read operations in a data storage retrieval system (see column 8 line 10) and having a cache memory, as per teachings of Ninomiya, would reduce read access time, thus providing a faster system.

Claim 49 is rejected under same rationale as claim 47 and 48.

Response to Amendment

Applicant's arguments filed February 21, 2004 have been fully considered but they are not deemed to be persuasive.

In response to applicant's argument on page 22 that states "There is nothing in the art, which suggest using a message network for passing messages together with a data transfer section having a cache memory coupled to a plurality of directors. In order to establish a prima facie case of obviousness, the combination claimed by the applicant must be suggested in the prior art itself. That is, the prior art must suggest or recognize or provide some motivation for the claimed combination. The Examiner has not pointed to anything in the prior art that suggests, recognizes, or provide some motivation to have a system with a message network for passing messages together with a data transfer section having a cache coupled to a plurality of directors. Thus it is respectfully submitted that the Examiner has not set forth a prima facie case of obviousness against any of the claims 34-46 and 48. Rather, the examiner seems to reach conclusion of obviousness from facts not in, nor supported by, the record ..... Further, why does adding a cache memory of Ninomiya to Martin's system run faster?" examiner respectfully disagrees.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). A cache memory, by definition (see Webster's dictionary), is a memory with very short access time used for storage of frequently used instructions or data. Thus, modifying Martin to incorporate a cache memory, as per teachings of Ninomiya, would provide a faster system because a cache would reduce read access time by storing frequently used data.

In response to applicant's argument on page 22 that states "Claim 40 points out that the messaging network passes messages from any of the first plurality of directors to a selected one of said second plurality of directors and from any one of the second plurality of directors to a selected one of the first plurality of directors," examiner respectfully disagrees. Martin discloses when a read or write is to be performed, the commanded IFS 14,16,18,or 20 (first plurality of resources) request resources from the CNS (messaging network) and the DRS 48 (second plurality of directors) is commanded throughout the read/write operation by that IFS (first plurality of directors) via a data channel through the SWS (messaging network).

Allowable Subject Matter

Claim 10,16,17,20,21,25, and 28 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8, 26, 32-39, 44-46, and 52-54 are allowable.

Examiner's Statement of Reason for Allowance

Claims 8, 26, 32-39, 44-46, and 52-54 are allowable over the prior art of records.

The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 8 and 26 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts.

The reason for allowance for claims 8, 26, 44, and 52 is the inclusion of messaging network comprising a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of directors, such network being operative independently of the data transfer section, in conjunction with the rest of the limitation set forth in the claim.

The reason for allowance for claims 32 and 53 is the inclusion of messaging network passes the messages from any one of the plurality of directors to a selected one of the plurality of directors and network being operative independently of the data transfer section, in conjunction with the rest of the limitation set forth in the claim.

The reason for allowance for claims 36 and 45 is the inclusion of messaging network passes the messages from any of the first plurality of directors to a selected one of said second plurality of directors and from any one of the second plurality of directors to a selected one of the first plurality of directors and network being operative independently of the data transfer section, in conjunction with the rest of the limitation set forth in the claim.

The remaining claims, not specifically mentioned, are allowed because they are dependent upon one of the claim mentioned above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Emerson Puente, whose telephone number is (703) 305-8012. The examiner can normally be reached on Monday-Friday from 8:00AM- 5:00PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Robert Beausoliel*, can be reached on *(703) 305-9713 or via e-mail addressed to [robert.beausoliel@uspto.gov]*. The fax number for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to **[emerson.puente@uspto.gov]**.

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 305-3900.

Emerson Puente
3/18/04

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100